WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

first and second access modes and an entry signal generation circuit for logically synthesizing a plurality of input signals to generate a first entry signal used to enter the first access mode; and

a control circuit connected to the entry signal generation circuit to generate a first mode trigger signal in response to the first entry signal, and when the control circuit receives a second entry signal to enter the second access mode, the control circuit generates a second mode trigger signal in response to the second entry signal;

wherein the entry signal generation circuit logically synthesizes the input signals in a selective manner in accordance with a selection control signal to generate the first entry signal.

2. The semiconductor memory device according to claim 1, wherein the selection control signal includes code information related to the logically synthesized input signals.

3. The semiconductor memory device according to claim 1, further comprising a test mode, wherein the selection control signal is provided to the entry signal generation circuit in the test mode, which is conducted in accordance with a test signal.

4. The semiconductor memory device according to claim 1, wherein the entry signal generation circuit includes:

a plurality of transition detectors, each detecting

transition of an associated one of the input signals to generate a detection signal; and

a pulse synthesizing circuit connected to the transition detectors to logically synthesize the detection signals in accordance with the selection control signal and generate the first entry signal.

5. The semiconductor memory device according to claim 1, further comprising a test mode, wherein the control circuit invalidates the second entry signal in accordance with a test signal used to enter the test mode and generates the second mode trigger signal in response to the first entry signal.

6. The semiconductor memory device according to claim 1, wherein the entry signal generation circuit logically synthesizes the input signals in accordance with the selection control signal and further generates a third entry signal used to enter the second access mode.

7. The semiconductor memory device according to claim 6, wherein the entry signal generation circuit includes:

a plurality of transition detectors, each detecting transition of an associated one of the input signals to generate a detection signal; and

a pulse synthesizing circuit connected to the transition detectors to logically synthesize the detection signals in accordance with the selection control signal and generate the first and third entry signals.

8. The semiconductor memory device according to claim 6, wherein the control circuit invalidates the second

entry signal in accordance with a test signal used to enter the test mode and generates the second mode trigger signal in response to the third entry signal.

9. The semiconductor memory device according to claim 6, wherein the control circuit includes:

a mode trigger generation circuit connected to the entry signal generation circuit to generate the first mode trigger signal in response to the first entry signal;

a determination circuit connected to the entry signal generation circuit to invalidate the second entry signal in accordance with the test signal and generate the second mode trigger signal in response to the third entry signal; and

an internal operation signal generation circuit connected to the mode trigger generation circuit and the determination circuit to generate an internal operation signal in accordance with the first mode trigger signal and the second mode trigger signal.

10. The semiconductor memory device according to claim 1, wherein the input signals include a plurality of control signals and a plurality of address signals.

11. The semiconductor memory device according to claim 1, further comprising a selection signal generation circuit connected to the entry signal generation circuit to generate the selection control signal.

12. The semiconductor memory device according to claim 1, further comprising a timer connected to the control circuit to generate the second entry signal.

13. The semiconductor memory device according to

claim 1, wherein the first access mode is a read operation mode or a write operation mode, and the second access mode is a self refresh operation mode.

14. A semiconductor memory device comprising:

first and second access modes and an entry signal generation circuit for logically synthesizing a plurality of input signals to generate an entry signal used to enter the first access mode or the second access mode; and

a control circuit connected to the entry signal generation circuit to generate a first mode trigger signal, which is used to start the first access mode, in response to the entry signal and to generate a second mode trigger signal, which is used to start the second access mode, in response to the entry signal;

wherein the entry signal generation circuit logically synthesizes the input signals in a selective manner in accordance with a predetermined selection control signal to inhibit the generation of the entry signal.

15. A semiconductor memory device comprising:

first and second access modes and an entry signal generation circuit for logically synthesizing a plurality of input signals to generate a first entry signal used to enter the first access mode and a second entry signal used to enter the second access mode; and

a control circuit connected to the entry signal generation circuit to generate a first mode trigger signal, which is used to start the first access mode, in response to the first entry signal and to generate a second mode trigger signal, which is used to start the second access mode, in response to the second entry signal;

wherein the entry signal generation circuit logically

synthesizes the input signals in a selective manner in accordance with a predetermined selection control signal to inhibit the generation of the first entry signal or the second entry signal.

16. A method for testing a semiconductor memory device having a first access mode, a second access mode, and a test mode, the method comprising:

receiving a test signal to enter the test mode;

receiving a plurality of input signals;

selecting at least one of the input signals and detecting transition of the selected at least one of the input signals; and

starting one of the access modes in accordance with the transition detection of the selected at least one of input signals.

17. The method according to claim 16, further comprising:

performing the other access mode in correspondence with the transition of the selected at least one of input signals after said one of the access modes is completed.

18. The method according to claim 17, further comprising:

performing said other access mode in correspondence with the transition of at least one of the input signals excluding the selected at least one of input signals.

19. The method according to claim 16, wherein the semiconductor memory device generates an access request signal, which requests entry of said one of the access modes, at predetermined time intervals, and the starting of said

one of the access modes includes invalidating the access request signal with the test signal.

20. A method for testing a semiconductor memory device having a first access mode and a second access mode, the method comprising:

receiving a plurality of input signals;

logically synthesizing the input signals to generate an entry signal used to enter the first access mode or the second access mode; and

logically synthesizing the input signals in a selective manner in accordance with the selection control signal to inhibit the generation of the entry signal.

21. A method for testing a semiconductor memory device having a first access mode and a second access mode, the method comprising:

receiving a plurality of input signals;

logically synthesizing the input signals to generate a first entry signal used to enter the first access mode;

logically synthesizing the input signals to generate a second entry signal used to enter the second access mode;

logically synthesizing the input signals in a selective manner in accordance with the selection control signal to inhibit the generation of the first entry signal or the second entry signal.